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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Morgan

Docket No.: TI-25995

Serial No.: 09/088,674

Art Unit: 2674

Filed: 2 June 1998

Examiner: Nguyen, Kevin M.

For: BOUNDARY DISPERSION FOR MITIGATING PWM TEMPORAL CONTOURING ARTIFACTS IN DIGITAL DISPLAYS

APPEAL BRIEF TRANSMITTAL

July 28, 2003

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner For Patents, PO Box 1450, Alexandria, Virginia 22313-1450 on the date below.

Charles A. Brill — 7-28-2003 Date

Transmitted herewith in triplicate is an Appeal Brief in the above-identified application.

Please charge the $320.00 fee for filing the Brief to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Charge any additional fees, or credit overpayment to Deposit Account No. 20-0668. Three copies of this sheet are enclosed.

Respectfully submitted,

Charles A. Brill
Attorney for Applicant(s)
Reg. No. 37,786

Texas Instruments Incorporated
P. O. Box 655474, MS 3999
Dallas, Texas 75265
Telephone: (972) 917-4379
Fax: (972) 917-4418

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APPEAL BRIEF UNDER 37 C.F.R. § 1.192

28 July 2003

Commissioner for Patents
P.O. Box 1450
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Charles A. Brill — 28 July 2003

Charles A. Brill — Date

Dear Sir:

The following Appeal Brief is respectfully submitted, in triplicate, in connection with the above-identified application in response to the Final Rejection mailed 28 February 2003, and the Advisory Action mailed 17 June 2003. Please charge all required fees to the deposit account of Texas Instruments Incorporated, Deposit Account 20-0668.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, to whom this application is assigned.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Applicant's legal representative.

STATUS OF THE CLAIMS

This application originally was filed 2 June 1998 with ten claims, two of which were written in independent form. Claims 1 and 6 were amended on 4 October 2000.

STATUS OF THE AMENDMENTS

An amendment to Claims 1 and 6 was filed on 4 October 2000. Additional responses not amending the claims were filed on 19 March 2001 and 10 September 2001. A response to the original final rejection was submitted on 19 February 2002 and an Appeal Brief was submitted on 3 June 2002. After prosecution was reopened, a response was filed 18 December 2002 and a response to the second final rejection was submitted 2 June 2003. All amendments to the claims have been entered.

SUMMARY OF THE INVENTION

One problem addressed by the current invention is described from line 22 of page 2 through line 16 of page 3 of the specification. Specifically, in real images, boundary conditions often exist where many display picture elements, or pixels, are spatially bunched together with similar image data. If the display system uses pulse width modulation (PWM) and the image data for the pixels has clusters of pixels that cross a major bit transition, PWM artifacts can occur.

The specification, from line 21 of page 3 through line 10 of page 5, provides a concise explanation of the invention defined in the appealed claims. One embodiment of the present invention offsets nominal pixel values alternately between a positive offset and a negative offset, repeatedly over a sequence of two display frames. The average

value of the two offset values over two displayed frames, as seen by the viewer, is equal to the nominal pixel value, while the PWM artifacts are reduced.

ISSUES

1. Whether Claim 1 is anticipated by U.S. Patent No. 5,053,764 to Barbier et al. under 35 U.S.C. § 102 (b).
2. Whether Claim 2 is anticipated by U.S. Patent No. 5,053,764 to Barbier et al. under 35 U.S.C. § 102 (b).
3. Whether Claim 3 is anticipated by U.S. Patent No. 5,053,764 to Barbier et al. under 35 U.S.C. § 102 (b).
4. Whether Claim 4 is anticipated by U.S. Patent No. 5,053,764 to Barbier et al. under 35 U.S.C. § 102 (b).
5. Whether Claim 6 is anticipated by U.S. Patent No. 5,053,764 to Barbier et al. under 35 U.S.C. § 102 (b).
6. Whether Claim 7 is anticipated by U.S. Patent No. 5,053,764 to Barbier et al. under 35 U.S.C. § 102 (b).
7. Whether Claim 8 is anticipated by U.S. Patent No. 5,053,764 to Barbier et al. under 35 U.S.C. § 102 (b).
8. Whether Claim 9 is anticipated by U.S. Patent No. 5,053,764 to Barbier et al. under 35 U.S.C. § 102 (b).

GROUPING OF THE CLAIMS

Claims 1-4 and 6-9 are independently patentable and stand or fall individually for the reasons more clearly set forth hereinbelow. Claim 5 stands or falls together with

Claim 1, from which Claim 5 depends. Claim 10 stands or falls together with Claim 6, from which Claim 10 depends.

ARGUMENTS

Issue 1:

Whether Claim 1 is anticipated by U.S. Patent No. 5,053,764 to Barbier et al. under 35 U.S.C. § 102 (b).

Claim 1 was rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,053,764 to Barbier et al. (Barbier). The applicant respectfully disagrees and submits the Examiner has failed to establish a prima facie case of anticipation under 35 U.S.C. § 102.

"A person shall be entitled to a patent unless," creates an initial presumption of patentability in favor of the applicant. 35 U.S.C. § 102. "We think the precise language of 35 U.S.C. § 102 that, "a person shall be entitled to a patent unless," concerning novelty and unobviousness, clearly places a burden of proof on the Patent Office which requires it to produce the factual basis for its rejection of an application under sections 102 and 103, see Graham and Adams." *In re Warner*, 379 F.2d 1011, 1016 (C.C.P.A. 1967) (referencing *Graham v. John Deere Co.*, 383 U.S. 1 (1966) and *United States v. Adams*, 383 U.S. 39 (1966)). "As adapted to *ex parte* procedure, *Graham* is interpreted as continuing to place the 'burden of proof on the Patent Office which requires it to produce the factual basis for its rejection of an application under sections 102 and 103'." *In re Piasecki*, 745 F.2d 1468 (Fed. Cir. 1984) (citing *In re Warner*, 379 F.2d at 1016).

"The prima facie case is a procedural tool which, as used in patent examination (as by courts in general), means not only that the evidence of the prior art would reasonably allow the conclusion the examiner seeks, but also that the prior art compels such a conclusion if the applicant produces no evidence or argument to rebut it." *In re Spada*, 911 F.2d 705, 708 n.3 (Fed. Cir. 1990).

The applicant respectfully submits the Examiner has failed to meet the burden of proof required to establish a prima facie case of anticipation. Section 2131 of the Manual of Patent Examiner's Procedure provides:

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. Of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053, (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as contained in the . . . claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim . . . . *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

With respect to independent Claim 1, the Examiner has failed to provide a prima facie case of anticipation because the Examiner failed to provide any teaching in Barbier of "offsetting a first pixel value a first predetermined amount to form a first offset pixel value and displaying said first offset pixel value during a first display frame; and offsetting said first pixel value by the opposite of said first predetermined amount to form a second offset pixel value and displaying said second offset pixel value during a second

display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value" as recited by Claim 1.

Barbier appears to teach, as stated in the abstract of Barbier, "The system enables the making of half-tones by using the control circuits of the matrix which are not usually designed for this purpose while producing no flicker effect. The system has a memory image with N (greater than or equal or 2) memory planes to store therein light information relating to each pixel in an N-bit word. The planes are read sequentially and thus make N-1 half-tones. In the simplest case (n=2), two planes are used and a first image is produced where any pixel is formed by a first bit, extracted from a first plane, and is preceded and followed, in rows as well as in columns, by a pixel formed by a first bit extraced [sic] from the other plane. The addressing is then determined to produce a second image by extracting, in reverse and respectively by each pixel, the second luminance bit in the other memory plane not used for the first image."

The Examiner stated, "As to claim 1, Barbier et al teaches a method of displaying digital image which includes a luminance state presenting a first interval 1/Fo around a mean value b+ (first offset value) and a second interval 1/Fo around a mean value b- (second offset value, col. 5, lines 9-12), the two different binary states of luminance a and b, a is the luminance level of a lit pixel (a first offset pixel value display frame), and b is the luminance level of an off pixel (the opposite/second offset pixel value display frame), the making of the semi-luminance (a+b)/2 (average of a displayed first offset pixel value and a second offset pixel value, figure 3 and 4, col. 5, lines 36-40)."

Figures 11A, 11B, 12A, and 12B of Barbier, coupled with the passages cited by the Examiner clearly show the error of this analysis. It is well known to apply

symmetrical excitation signals to liquid crystal displays (col. 5, lines 4-8). The display of Barbier is capable of displaying two levels, an excited level represented in Figures 12A and 12B, and an un-excited level represented in Figures 11A and 11B. In each figure, the "A" portion shows the voltage V_E applied to the pixel, and the "B" portion shows the corresponding luminance (col. 5, lines 8-16).

The Examiner appears to claim that levels b+ and b- are somehow the offset pixel values recited by Claim 1. Barbier teaches, however, that b+ and b- are the actual luminance levels produced by the pixel using a constant excitation voltage (0 in the case of an un-excited pixel). The periodic variance of the illumination level appears to be due to the addressing circuitry chosen by Barbier to address a liquid crystal panel. Likewise, when the image data specifies an excited pixel, Barbier applies an alternating V+ V- voltage to the pixel to yield a luminance that varies about a+ during the V+ portion and a- during the V- portion.

The ripple in luminance shown in Figures 11B and 12B cannot be interpreted as the result of a first and second offset pixel value, but are the result of the means Barbier uses to drive the liquid crystal panel—and which Barbier attempts to limit (col. 5, lines 21-49). Barbier states "the imperfection of the circuitry addressing each cell leads to slight luminance ripple especially at high incidence of observation between two successive addressing stages" (col. 5, lines 24-27).

The Examiner refers to Figures 3 and 4 and the semi-luminance (a+b)/2 as the average of a first offset pixel value and a second offset pixel value. The applicant respectfully submits this is taking Barbier completely out of context. Figures 3 and 4 are described by Barbier in column 3. Barbier teaches a system in column 3 in which "the

luminance is codified in a two-bit word and where the memory 5 has two planes." (col. 3, lines 9-10. Barbier refers to the binary luminance bit stored in memory plane A as a first bit a, and the binary luminance bit stored in memory plane B as a second bit b. The "a" and "b" referenced in Figures 3 and 4 do not appear to be related to the a+, a-, b+, and b- luminance levels discussed earlier, but merely denote in which memory plane a bit is stored. As shown in Figures 3 and 4, Barbier displays data from each of the two memory planes in a first and second display period. As Barbier states, "This system can thus be used, when a and b are equal, to produce a mean state equal to '1' or a mean state equal to '0' . . . The system further makes it possible to produce a third state which is the half tone '½' corresponding to the case where the values a and b are distinct, one being equal to '1' while the other is equal to '0'."

In summary, Examiner combined Barbier's varying luminance levels "a+," "a-," "b+," and "b-," with Barbier's use of data "a" and "b" from multiple memory planes "A" and "B," but has failed to show any teaching of Barbier that fairly shows, teaches, or suggests the recited limitations of Claim 1, namely, "offsetting a first pixel value a first predetermined amount to form a first offset pixel value and displaying said first offset pixel value during a first display frame; and offsetting said first pixel value by the opposite of said first predetermined amount to form a second offset pixel value and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value." The Examiner has therefore failed to present a prima facie case of anticipation and the applicant requests the Board of Patent Appeals and Interferences to reverse the Examiner's rejection.

Issue 2:

Whether Claim 2 is anticipated by U.S. Patent No. 5,053,764 to Barbier et al. under 35 U.S.C. § 102 (b).

The applicant respectfully submits the Examiner has failed to establish a prima facie case of anticipation under 35 U.S.C. § 102 of Claim 2.

The Examiner stated, "Barbier et al teaches a luminance state presenting a first interval 1/FO around a mean value b+ (first predetermined amount, col. 5, lines 10-11)." The applicant respectfully submits that not only does Barbier fail to show, teach, or suggest the limitations of the independent claim as argued above, the Examiner has failed to address the further limitation, "wherein the value of said first predetermined amount is selected as a function of said first pixel value" of Claim 2. The Examiner has therefore failed to present a prima facie case of anticipation and the applicant requests the Board of Patent Appeals and Interferences to reverse the Examiner's rejection.

Issue 3:

Whether Claim 3 is anticipated by U.S. Patent No. 5,053,764 to Barbier et al. under 35 U.S.C. § 102 (b).

The applicant respectfully submits the Examiner has failed to establish a prima facie case of anticipation under 35 U.S.C. § 102 of Claim 3.

The Examiner stated, "Barbier et al teaches a luminance state presenting a first interval 1/FO around a mean value b+ (first offset value b+ is greater than a first pixel value b, col. 5, lines 9-12)." The applicant respectfully submits that not only does Barbier fail to show, teach, or suggest the limitations of the independent claim, the

Examiner has failed to address the further limitation, "wherein said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed" of Claim 3. The Examiner has therefore failed to present a prima facie case of anticipation and the applicant requests the Board of Patent Appeals and Interferences to reverse the Examiner's rejection.

Issue 4:

Whether Claim 4 is anticipated by U.S. Patent No. 5,053,764 to Barbier et al. under 35 U.S.C. § 102 (b).

The applicant respectfully submits the Examiner has failed to establish a prima facie case of anticipation under 35 U.S.C. § 102 of Claim 4.

The Examiner stated, "Barbier et al teaches the pixels value a and b extracting from a plurality of weight-bit plane A1, A2 and B1, B2 (col. 3, lines 52-59)." The applicant respectfully submits that not only does Barbier fail to show, teach, or suggest the limitations of the independent claim, the Examiner has failed to address the further limitation, "said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame" of Claim 4. The Examiner has therefore failed to present a prima facie case of anticipation and the applicant requests the Board of Patent Appeals and Interferences to reverse the Examiner's rejection.

Issue 5:

Whether Claim 6 is anticipated by U.S. Patent No. 5,053,764 to Barbier et al. under 35 U.S.C. § 102 (b).

The applicant respectfully submits the Examiner has failed to establish a prima facie case of anticipation under 35 U.S.C. § 102 of Claim 6 because the Examiner failed to provide any teaching in Barbier of "a logic circuit offsetting a first pixel value a first predetermined amount to form a first offset pixel value, said logic circuit also offsetting said first said pixel value by the opposite of said first predetermined amount to form a second offset pixel value; and display means displaying said first offset pixel value during a first display frame and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value" as recited by Claim 6.

The Examiner stated, "Barbier et al teaches a system of displaying digital image which includes a graphic processor 2 (logic circuit) controlling/offsetting by a processor 1 (figure 1, col. 3, lines 1-3), a luminance state presenting a first interval 1/FO around a mean value b+ (first offset value) and a second interval 1/FO around a mean value b- (second offset value, col. 5, lines 9-12), a display screen 11 (col. 3, lines 4-6) displays the two different binary states of luminance a and b, a is the luminance level of a lit pixel (a first offset pixel value display frame), and b is the luminance level of an off pixel (the opposite/second offset pixel value display frame), the making of the semi-luminance (a+b)/2 (average of a displayed first offset pixel value and a second offset pixel value, figure 3 and 4, col. 5, lines 36-40)."

The applicant submits the teachings of Barbier, as discussed above with respect to Claim 1, simply do not support the Examiner's transformation of Barbier's display of multiple bit planes, which contain image data associated with both lit and un-lit pixels, into the system described by applicant's Claim 6. The Examiner has failed to point to

any teaching in Barbier of "offsetting a first pixel value a first predetermined amount to form a first offset pixel value, said logic circuit also offsetting said first said pixel value by the opposite of said first predetermined amount to form a second offset pixel value" as recited by Claim 6. The Examiner has therefore failed to present a prima facie case of anticipation and the applicant requests the Board of Patent Appeals and Interferences to reverse the Examiner's rejection.

Issue 6:

Whether Claim 7 is anticipated by U.S. Patent No. 5,053,764 to Barbier et al. under 35 U.S.C. § 102 (b).

The Examiner stated, "Barbier et al teaches a graphic processor 2 controlling a luminance state presenting a first interval 1/FO around a mean value b+ (first predetermined amount, col. 5, lines 10-11)." The applicant respectfully submits that not only does Barbier fail to show, teach, or suggest the limitations of the independent claim, the Examiner has failed to address the further limitation, "the value of said first predetermined amount is selected by said logic circuit as a function of said first pixel value" of Claim 7. The Examiner has therefore failed to present a prima facie case of anticipation and the applicant requests the Board of Patent Appeals and Interferences to reverse the Examiner's rejection.

Issue 7:

Whether Claim 8 is anticipated by U.S. Patent No. 5,053,764 to Barbier et al. under 35 U.S.C. § 102 (b).

The Examiner stated, "Barbier et al teaches a graphic processor 2 controlling a luminance state presenting a first interval 1/FO around a mean value b+ (first offset value

b+ is greater than a first pixel value b, col. 5, lines 9-12)." The applicant respectfully submits that not only does Barbier fail to show, teach, or suggest the limitations of the independent claim, the Examiner has failed to address the further limitation, "said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed" of Claim 8. The Examiner has therefore failed to present a prima facie case of anticipation and the applicant requests the Board of Patent Appeals and Interferences to reverse the Examiner's rejection.

Issue 8:

Whether Claim 9 is anticipated by U.S. Patent No. 5,053,764 to Barbier et al. under 35 U.S.C. § 102 (b).

The Examiner stated, "Barbier et al teaches a graphic processor 2 controlling the pixels value a and b extracting from a plurality of weight-bit plane A1, B1 and A2, B2 (col. 3, lines 52-59)." The applicant respectfully submits that not only does Barbier fail to show, teach, or suggest the limitations of the independent claim, the Examiner has failed to address the further limitation, "said pixel values are displayed using a plurality of weighted bit-planes, wherein said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame" of Claim 9. The Examiner has therefore failed to present a prima facie case of anticipation and the applicant requests the Board of Patent Appeals and Interferences to reverse the Examiner's rejection.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-10 under 35 U.S.C. § 102 as being anticipated by Barbier is

improper, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejection.

Please charge any fees necessary in connection with the filing of this paper, including any necessary extension of time fees, to Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,

Charles A. Brill
Attorney for Applicant
Reg. No. 37,786

Texas Instruments Incorporated
P.O. Box 655474 M/S 399
Dallas, TX 75265
(972) 917-4379
FAX: (972) 917-4418

APPENDIX

1. (amended) A method of displaying digital video data comprising pixel values, said method comprising the steps of:

   offsetting a first pixel value a first predetermined amount to form a first offset pixel value and displaying said first offset pixel value during a first display frame; and

   offsetting said first pixel value by the opposite of said first predetermined amount to form a second offset pixel value and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value.

2. The method as specified in Claim 1 wherein the value of said first predetermined amount is selected as a function of said first pixel value.

3. The method as specified in Claim 1 wherein said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed.

4. The method as specified in Claim 1 wherein said pixel values are displayed using a plurality of weighted bit-planes, wherein said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame.

5. The method as specified in Claim 1 wherein said first display frame and said second display frame are consecutive.

6. (amended) A system of displaying digital video data comprising pixel values,

comprising:

a logic circuit offsetting a first pixel value a first predetermined amount to form a first offset pixel value, said logic circuit also offsetting said first said pixel value by the opposite of said first predetermined amount to form a second offset pixel value; and

display means displaying said first offset pixel value during a first display frame and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value.

7. The system as specified in Claim 6 wherein the value of said first predetermined amount is selected by said logic circuit as a function of said first pixel value.

8. The system as specified in Claim 6 wherein said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed.

9. The system as specified in Claim 6 wherein said pixel values are displayed using a plurality of weighted bit-planes, wherein said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame.

10. The system as specified in Claim 6 wherein said first display frame and said second display frame are consecutive.